and the like, the subject matter described herein is not limited to those technologies, and, as such, can be used with other radio technologies as well.

[0052] Although a few variations have been described in detail above, other modifications or additions are possible. In particular, further features and/or variations may be provided in addition to those set forth herein. Moreover, the example embodiments described above may be directed to various combinations and subcombinations of the disclosed features and/or combinations and subcombinations of several further features disclosed above. In addition, the logic flow depicted in the accompanying figures and/or described herein does not require the particular order shown, or sequential order, to achieve desirable results. Other embodiments may be within the scope of the following claims.

What is claimed:

1. An apparatus comprising:

an envelope detector to track an envelope of a signal being amplified by an amplifier;

a first direct-current to direct-current converter supplying power to the amplifier, the power supplied by the first direct-current to direct-current converter including one or more high-frequency components of the envelope tracked by the envelope detector; and

a second direct-current to direct-current converter supplying power to the amplifier, the power supplied by the second direct-current to direct-current converter including one or more low-frequency components of the envelope tracked by the envelope detector.

2. The apparatus of claim **1** further comprising:

a power amplifier coupled to the envelope detector, the first direct-current to direct-current converter, and the second direct-current to direct-current converter

3. The apparatus of claim **1**, wherein the first direct-current to direct-current converter is characterized by a frequency response defined at least in part by at least one of a width of a transistor and a fast ramp voltage.

4. The apparatus of claim **3**, wherein the width comprises between about 500 microns and about 1000 microns in a 65 nanometer semiconductor process.

5. The apparatus of claim **1**, wherein the second direct-current to direct-current converter is characterized by a frequency response defined at least in part by at least one of a width of a transistor and a slow ramp voltage.

6. The apparatus of claim **5**, wherein the width comprises between about 5 millimeters and about 10 millimeters in a 65 nanometer semiconductor process.

7. The apparatus of claim **1**, wherein a wireless user equipment includes the apparatus.

8. A non-transitory computer-readable medium encoded with instructions that, when executed by at least one processor, cause at least the following:

tracking, by an envelope detector, an envelope of a signal being amplified by an amplifier;

supplying, by a first direct-current to direct-current converter, power to the amplifier, the power supplied by the first direct-current to direct-current converter including one or more high-frequency components of the envelope tracked by the envelope detector; and

supplying, by a second direct-current to direct-current converter, power to the amplifier, the power supplied by the second direct-current to direct-current converter including one or more low-frequency components of the envelope tracked by the envelope detector.

9. The non-transitory computer-readable medium of claim **8** further comprising:

a power amplifier coupled to the envelope detector, the first direct-current to direct-current converter, and the second direct-current to direct-current converter.

10. The non-transitory computer-readable medium of claim **8**, wherein the first direct-current to direct-current converter is characterized by a frequency response defined at least in part by at least one of a width of a transistor and a fast ramp voltage.

11. The non-transitory computer-readable medium of claim **10**, wherein the width comprises between about 500 microns and about 1000 microns in a 65 nanometer semiconductor process.

12. The non-transitory computer-readable medium of claim **8**, wherein the second direct-current to direct-current converter is characterized by a frequency response defined at least in part by at least one of a width of a transistor and a slow ramp voltage.

13. The non-transitory computer-readable medium of claim **12**, wherein the width comprises between about 5 millimeters and about 10 millimeters in a 65 nanometer semiconductor process.

14. The non-transitory computer-readable medium of claim **8**, wherein a wireless user equipment includes the envelope detector, the first direct-current to direct-current converter, and the second direct-current to direct-current converter.

15. An method comprising:

tracking, by an envelope detector, an envelope of a signal being amplified by an amplifier;

supplying, by a first direct-current to direct-current converter, power to the amplifier, the power supplied by the first direct-current to direct-current converter including one or more high-frequency components of the envelope tracked by the envelope detector; and

supplying, by a second direct-current to direct-current converter, power to the amplifier, the power supplied by the second direct-current to direct-current converter including one or more low-frequency components of the envelope tracked by the envelope detector.

16. The method of claim **15** further comprising:

a power amplifier coupled to the envelope detector, the first direct-current to direct-current converter, and the second direct-current to direct-current converter.

17. The method of claim **15**, wherein the first direct-current to direct-current converter is characterized by a frequency response defined at least in part by at least one of a width of a transistor and a fast ramp voltage.

18. The method of claim **17**, wherein the width comprises between about 500 microns and about 1000 microns in a 65 nanometer semiconductor process.

19. The method of claim **15**, wherein the second direct-current to direct-current converter is characterized by a frequency response defined at least in part by at least one of a width of a transistor and a slow ramp voltage.

20. The method of claim **19**, wherein the width comprises between about 5 millimeters and about 10 millimeters in a 65 nanometer semiconductor process.

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